

Future microcontrollers

8/16 bit

pins	Flash
8	1/2/4K
14	2/4/8K
20	4/8/16K
28	8/16/32K

Circular buffers for better determination of logical inputs states. 100Ω on inputs to absorb energy.
Result in register or memory. Cpu frequency = $f/4, /2, \times 1, \times 2$. Fixed peripheral frequency.
Banks of flash. Each contains either instructions or data (simultaneous addressing). 16 bit data path.

≤ 32KB : 4 8 bit registers (Ai, Xi). 9x128B direct addressing. 16, 16/32 bit instructions.

Ex : LDA (XX)+ MOV #XX,(Xi) ADX #XX DJNZ R,XX CLR XX ADD A0,XX,d
SHL Ri,XX CMP Xn,Xn' CPX XX JSR XXX TJZ #XX,Ri,xXXX JBC XX,n,xXXX

16/32 bit

pins	Flash	// link
32	16/24/32/48K	4 bit
48	32/48/64/96K	8 bit
64	64/128/256K	8 bit
80	128/256/512	16 bit
100	256/512K/1M	16 bit
120	512K/1/2/4M	16 bit
144	2/4/8/16M	32 bit

≤ 96K: 16 8 bit registers. 4KB direct addressing. 24 bit instructions. Ex: CMP X,XXX JEQ XXXX

≤ 2M : 32 ports & 16 16 bit registers. 80KB direct addressing. 16/32 bit instructions. Ex : BSET Xn
ADD X,X AND X,X,#XXXXX CMP xX,XXXXX TJZ xX,XXXXX MOV #XX,XXXXX

≤ 2MB : 256 8 bit ports & registers. 64/80KB direct addressing. 8/16 bit link : 1T/256T x 256B
32/64 bit instructions. Ex : JBS xX,n,XXXXX ADD XX,XX,#XX MOV #XX,XXXXX
AV XX,XX,XX ADD XX,XXXXX TJZ XX,XXXXX CMP XX,#XXXXX

≥ 4M: (Dual) 32+2x16 16 bit registers. 2 RAM. 640KB direct addressing. (2x)32/64 bit instructions

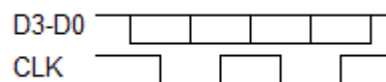
Ex : ADD xX,xX,#XXXXX MOV #X,XXXXX CMP xX,XXXXX TJZ xX,XXXXX

Romless : 2x256 16 bit registers. 16MB addressing. Complex numbers. 32/64/96 bit instructions.

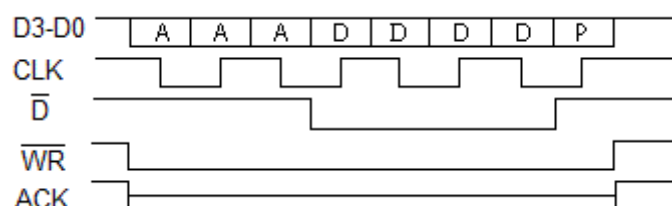
Ex : ADD XX,#XXXXX INC XXXXXX AND XXXXXX,XX,#XXXXX JMP xXXXXXX

4 bit link :

Can access to 4 slaves at a time. 16 bit read/write in single mode :



16 bit write in extended mode :



Dual 32/64 bit

2x4096 8 bit registers. 2x64/128 bit instructions. 64 bit ex : CJEQ XXX,XXX,XXXX.XXXX

Instructions for cooperative multitasking :

OPEN XX : Open and go to a new subroutine, starting at the specified address.

NEXT XX : Go to the next programs, then come back at the indicated address.

END : Wait for subroutines end. KILL : end of subroutine.

Semi-software management for data cache :

BLD 100.0000 : Load in cache, the 16 bytes block of external memory, from address 1.0000.0000, if it's not already done.

BLO 100.0000 : Bulk load only (MSB = 1 : Read only). Written or LRU block erased.

RES 100.0000 : Reserve a location in cache, for writing from 1.0000.0000.

BST 100.0000 : Store modified block of 256 bytes, in external memory block, from address 1.0000.0000, if writing is possible and allowed and if it's not already done.

Serial module :

- (Differential) half or full-duplex, modulated or not asynchronous serial link.
- 8 bit synchronous serial link active low to high and high to low edges. $f / (n+2)$.
- Normal or open drain output(s). Slave select input or conditional clock outputs.
- Integrated multiplexer. Possibility of keyboard reading (3 pins: Clock, Reset, Key_Pressed).

Analog module :

- 8 modes including comparisons or 2 simultaneous conversions (2 msb ... 2 lsb).
- Linear 8 to 12 bit or logarithmic 8 bit. Single ended or differential conversion.
- Brushless position decoder from hall sensors. 2.56V or 4096 mV internal reference.
- Comparator can limit current with PWM pins after time out.
- Possibility of filtering values to make a 24 bit delta-sigma conversion.
- Possibility of sampling with clock stopped and sleeping during conversion.
- Possibility of two complementary or independent analog outputs.
- Possibility of automatic transmitting analog conversion result on external link.

2 ADC	24 DAC	24 CMP	12x2 DAC
1 ADC + 12 DAC	12 DAC + 12 CMP	12 CMP + 1 ADC	12x2 CMP

Timer

PPM, internal or external frequency divider. Linear or logarithmic counter.

Sleep for, until / Watchdog of / Interrupt every 2 μ s to 131 ms.

PWM : Switching between 2 nibbles with automatic period adjustment :

α	T
<1/128	8192
<1/32	4096
<1/8	2048
<7/8	1024